APPENDIX A (STATUS)

14. (Canceled) The process of preventing high electric field concentration in a surface of a dielectric body at a facetted shaped intersection with sub 250 nanometer range size and spacing conductive interconnect members in said dielectric body, comprising the step of:

positioning a mask member of a material that is hardened relative to the hardness of said dielectric body surrounding at least one said conductive interconnect member and over at least a portion of said dielectric member at a location below said surface at distance defined by the beginning of said facetted portion.

15. (Currently Amended) The process of claim ~~14~~ 22 wherein the material of said mask ~~member~~ layer is a material taken from the group of amorphous silicon, carbon, hydrogen(-Si:C:H); silicon, carbon, oxygen, hydrogen alloys (organosiloxane or Si:C:O:H); silicon, nitrogen, carbon alloys (SiLN:C); silicon nitride (Si_3N_4); silicon dioxide (SiO_2); and silicon oxynitride (SiON).

16. (Canceled) In a process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric to a common surface,

an improvement comprising the intermediate steps of:

depositing a diffusion barrier liner in the formation of said conductive interconnect members where said conductive interconnect members pass through said bulk dielectric, and then employing said diffusion barrier liner as the conductor for plating in subsequent deposition of metal filling said conductive interconnect members.

17. (Currently Amended) The process improvement of claim 16 wherein the material of diffusion barrier liner is a material taken from the group of at least one of Ta, Ti, TaN, TiN, W, and WN, and said subsequently deposited metal is copper.~~[.]~~

18. (Currently Amended) The process of fabricating sub 250 nanometer size and spacing semiconductor device interconnections wherein conductive interconnect members pass through a portion of a bulk dielectric and through a mask to a mask layer atop said dielectric to a common surface,

an improvement comprising the intermediate steps of:

etching trench and via shape openings out of said dielectric body through said mask layer in a region below said surface,

lining said openings with a thin electrically conductive diffusion barrier layer,

coating said liner layer with a thin metal layer,

electroplating a thick metal into and filling said openings including overcoating said surface,

planarizing said overcoated surface through chemical-mechanical operations, and

removing said mask layer in all portions between said openings to a depth that establishes a selected dimension of the upper surface of said mask below said surface;

<u>depositing a protective cap film on exposed overcoated surface and remaining exposed surface, said cap film minimizing leakage and improving electrical reliability.</u>

19. (Currently Amended) The process of claim 18 wherein said mask member is of at least one material taken from the group of amorphous silicon, carbon, hydrogen(α – Si:C:H); silicon, carbon, oxygen, hydrogen alloys (organosiloxane or Si:C:O:H); silicon, nitrogen, carbon alloys (SiLN:C); silicon nitride (Si_3N_4); silicon dioxide (SiO_2); and silicon oxynitride (SiON).

20. (Currently Amended) The process of claim 19 wherein said thin electrically conducting diffusion barrier liner is a material taken fronm the group of at least one of Ta, Ti, TaN, TiN, W, and WN, and said subsequently deposited metal is copper[,].

21. (Currently Amended) The process of claim 20 wherein said thick metal being electroplated into and filling said openings is of at least one metal taken from the groups of copper, aluminum, silver, gold and alloys thereof.

22. New) The process of preventing high electric field concentration in a surface of a dielectric body at a facetted shaped intersection with sub 250 nanometer range size and spacing conductive interconnect members in said dielectric body, comprising the steps of:
depositing a bulk layer of intralevel dielectric material on a silicon substrate;
etching, using a mask layer, via and trench openings as used in damascene structures, the mask layer formed of a material that is hardened relative to the hardness of said dielectric body, which surrounds a conductive layer and which has an upper surface;
coating said etched openings with conductive diffusion barrier liners using a vapor deposition procedure selected from the group consisting of chemical or physical methods, said liner serving as an adhesion barrier between said intralevel dielectric and a thin copper layer, said liner also

acting as an electroplating conductor;

electroplating and filling said etched openings with additional copper to form copper conductors;

polishing using chemical or mechanical means so that said copper conductors are nearly coplanar with said upper mask surface;

removing said liner;

removing said mask layer in all portions between said etched openings to a depth that establishes a selected dimension of the upper surface of said mask below said surface;

depositing a protective cap film on exposed overcoated surface and remaining exposed surface, said cap film minimizing leakage and improving electrical reliability.